

Claims:

1    1.    A system to initiate, by a host, an event in a first device, the system comprising:  
2                 a signal line to communicate a plurality of data values between a host and one or more  
3         second devices; and  
4                 a tap line to communicate said plurality of data values between said signal line and said  
5         first device;  
6                 wherein said event is initiated upon detection, by said first device, of a predetermined  
7         sequence of data values on the tap line.

Q1    2.    The system of claim 1, wherein the event comprises a switching from a communication  
Q2         path between the first device and a third device and a communication path between the signal  
Q3         line and the third device.

Q1    3.    The system of claim 1, wherein the event comprises a switching from a communication  
Q2         path between a signal line and a third device and a communication path between the first device  
Q3         and the third device.

1    4.    The system of claim 1, wherein the host is a processor.

1    5.    The system of claim 1, wherein the first device is a logic device.

1    6.    The system of claim 1, wherein each of the one or more second devices is a memory  
2         device.

- 1      7.     The system of claim 1, wherein the third device is a memory device.
- 1      8.     The system of claim 1, wherein the host is a microprocessor chipset, the first device is a  
2     Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-  
3     line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access  
4     Memory (SDRAM).
- 1      9.     The system of claim 1, wherein each of the plurality of data values represents a memory  
2     location within any of the plurality of second memory devices.
- 1      10.    The system of claim 9, wherein utilization of a data value provides a call to the  
2     represented memory location.
- 1      11.    A method to initiate, by a host, an event in a first device comprising:  
2                communicating, by a signal line, a plurality of data values between a host and one or  
3     more second devices;  
4                communicating, by a tap line, said plurality of data values between said signal line and  
5     said first device; and  
6                initiating said event upon detection by said first device of a predetermined sequence of  
7     data values on the tap line.

1       12.     The method of claim 11, wherein the event comprises a switching from a communication  
2     path between the first device and a third device and a communication path between the signal  
3     line and the third device.

1       13.     The method of claim 11, wherein the event comprises a switching from a communication  
2     path between a signal line and a third device and a communication path between the first device  
3     and the third device.

1       14.     The method of claim 11, wherein the host is a processor.

1       15.     The method of claim 11, wherein the first device is a logic device.

1       16.     The method of claim 11, wherein each of the one or more second devices is a memory  
device.

1       17.     The method of claim 11, wherein the third device is a memory device.

1       18.     The method of claim 11, wherein the host is a microprocessor chipset, the first device is a  
2     Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-  
3     line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access  
4     Memory (SDRAM).

1       19.     The method of claim 11, wherein each of the plurality of data values represents a memory  
2     location within any of the plurality of second memory devices.

1       20.     The method of claim 19, wherein utilization of a data value provides a call to the  
2     represented memory location.

1       21.     A set of instructions residing in a storage medium, said set of instructions capable of  
2     being executed by a processor to initiate, by a host, an event in a first device comprising:  
3                 communicating, by a signal line, a plurality of data values between a host and one or  
4     more second devices;

5                 communicating, by a tap line, said plurality of data values between said signal line and  
6     said first device; and

7                 initiating said event upon detection by said first device of a predetermined sequence of  
8     data values on the tap line.

9       22.     The set of instructions of claim 21, wherein the event comprises a switching from a  
1     communication path between the first device and a third device and a communication path  
2     between the signal line and the third device.

3       23.     The set of instructions of claim 21, wherein the event comprises a switching from a  
4     communication path between a signal line and a third device and a communication path between  
5     the first device and the third device.

- 1    24.    The set of instructions of claim 21, wherein the host is a processor.
- 1    25.    The set of instructions of claim 21, wherein the first device is a logic device.
- 1    26.    The set of instructions of claim 21, wherein each of the one or more second devices is a  
2    memory device.
- 1    27.    The set of instructions of claim 21, wherein the third device is a memory device.
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